Boosting Machine Vision with Built-in FPGA Image Preprocessing

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Machine vision has been widely adopted for automatic inspection in industrial production environments to improve quality, reliability, stability, consistency and efficiency over conventional visual inspection by operators. Since image processing tasks can consume major CPU resources in machine vision applications, increasing processing performance within size constraints is, accordingly, a common challenge for solution providers. One option that is often overlooked in machine vision solutions is the FPGA, which can help address such performance shortcomings.

Challenges of Machine Vision Solutions

Currently, in order to fulfill user needs, effective machine vision systems are required to address the following user requirements, despite some contradictory aspects.
• **Compact size:** Machine vision system designers and developers must accommodate other equipment and structures in the production environment, with available space for the deployment of the machine vision system frequently limited.

• **Maximum resolution & frame rate:** In many cases, automatic inspection systems must utilize miniaturized components for defect detection operations, whereby even higher image resolution is required for accurate inspection, with higher frame rates needed to speed inspection and boost throughput.

• **Increased processing performance:** Higher resolutions and frame rates demand that vision systems be capable of managing large volumes of image frame data flow to inspect for defects.

• **Ease-of-use:** Vision systems with easy operation provide clear benefits in convenience and reduced programming demands. For system developers, reduced system footprint and I/O complexity significantly ease installation and deployment efforts, as do minimized programming requirements through use of a familiar programming environment.

“**One option that is often overlooked in machine vision solutions is the FPGA…”**

**Vision System Selection**

While conventional machine vision solutions have relied on high-performance CPUs, coordinated with image processing software, to achieve requisite speed and quality in image processing applications, such powerful processors tend to be more expensive and require larger, more complex systems. The IPC-based solutions often utilize a standalone industrial PC to connect cameras with an external line via external or embedded frame grabbers (See Figures 1 & 2).

<table>
<thead>
<tr>
<th></th>
<th>Conventional Smart camera</th>
<th>New Generation Smart camera</th>
<th>IPC-based Vision System</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td>Intel Atom Z530</td>
<td>Intel Atom E3845</td>
<td>Intel Core i7-3610QM</td>
</tr>
<tr>
<td></td>
<td>@ 1.60GHz</td>
<td>@ 1.91GHz</td>
<td>@ 2.30GHz</td>
</tr>
<tr>
<td><strong># of Physical Cores</strong></td>
<td>1</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td><strong>Max TDP</strong></td>
<td>2W</td>
<td>10W</td>
<td>45W</td>
</tr>
<tr>
<td><strong>CPU Mark</strong></td>
<td>281</td>
<td>1403</td>
<td>7462</td>
</tr>
<tr>
<td><strong>Footprint</strong></td>
<td>Small</td>
<td>Small</td>
<td>Large</td>
</tr>
</tbody>
</table>

Table 1: Comparison of smart camera solutions for vision systems


*Source: 2010 AIA annual machine vision market report.*
Graphic-intensive applications, such as industrial vision systems, that routinely process large amounts of data rely heavily on CPU performance. Inherent conflicts can result when the high performance is delivered at the expense of system size and cost conservation. Intense processing by the already more expensive CPU requires more power and generates increased heat, requiring a larger and more powerful system for dissipation.

As noted, it has previously been a distinct challenge to benefit from the advantages of industrial vision systems while balancing performance and size goals. The introduction of FPGAs (field-programmable gate arrays) into the system is a method of overcoming these challenges that are currently receiving considerable attention.

Advantages of FPGA

FPGAs are reprogrammable circuits utilizing parallel computing architecture and consist of multiple configurable logic blocks (CLBs), fixed function logic blocks and embedded RAM. With FPGAs, computing tasks are developed with a configuration file that dictates how components are interconnected. Using prebuilt logic blocks and programmable routing resources, an FPGA can be configured to implement custom hardware function without the need for the time-consuming and complicated PCB (printed circuit board) fabrication process of custom ASIC design. As FPGAs are completely reconfigurable, they take on a different functional identity every time the file is recompiled to dictate new circuitry configuration.

Delivering hardware-based speed and reliability while retaining superior application flexibility, FPGAs combine the best of ASICs and processor-based systems resulting in popularity across many industry segments. Semiconductor processing, for example, often employs FPGAs for product prototyping, in which ideas or trial capabilities can be tested and verified in hardware without the expense and difficulty of a complete chip fabrication process.
The FPGA’s fully parallel nature allows each independent processing task to be assigned to a dedicated section of the chip. Processing operations of the section are isolated from other logic blocks so the performance of the section is unaffected when more processing tasks are added. Consequently, FPGAs handily manage multiple tasks at the same time and at maximum processing speeds, making them particularly suited for implementation of data-intensive processing for parallel algorithms.

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Significant benefits of FPGAs include:

- **Boosted performance**: Hardware parallelism enables FPGAs to outperform CPUs in processing certain algorithms, especially those of a parallel nature, as much as thousands of times faster.

- **Faster time-to-market**: With FPGAs, reprogrammability allows ideas or trial capabilities to be tested and verified in hardware without the time, expense and difficulty of a complete chip fabrication process. Changes can be made or discarded, and retested within hours instead of weeks, therefore radically reducing product development time and expenditure.

- **Reducing cost**: Without the engineering (NRE) expenses of custom ASICs, FPGAs are extremely cost-efficient, not only for product prototyping but also system upgrades and expansion. Incremental changes to FPGA design to increase and improve functionality meeting new system requirements can be simply and inexpensively accomplished with no need to re-spin a board. Also since FPGAs are field-upgradeable, they typically provide a longer service life with reduced long-term maintenance costs.

Using an FPGA chip as co-processor to implement selected image processing algorithms can help offload CPU tasking, freeing resources to perform other operations. Image data can be streamed between FPGA and CPU to facilitate concurrent function, boosting overall performance of the vision system dramatically.

**CPU vs. FPGA Performance Comparison**

As shown, a CPU-based operation takes 4.5 ms and uses 4% of resources for a commonly used image processing utility to process an LUT algorithm on a 2 Mpixel image (see Figure 3). FPGA, conversely, completes the same task in only 25 ns without using any CPU resources, representing a 100,000X
increase in speed. Further, when performing shading correction functions, the CPU with image processing software takes 1.3 ms and 2% of CPU resources to complete, compared with a time of 25 ns with zero CPU usage by an FPGA.

**CPU vs. FPGA Performance Comparison**

<table>
<thead>
<tr>
<th>2 Mega pixel image</th>
<th>Halcon</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUT</td>
<td>1.8ms</td>
<td>25ns</td>
</tr>
<tr>
<td>LUT CPU resource</td>
<td>4%</td>
<td>0%</td>
</tr>
<tr>
<td>Shading correction</td>
<td>0.3ms</td>
<td>25ns</td>
</tr>
<tr>
<td>Shading correction CPU resource</td>
<td>2%</td>
<td>0%</td>
</tr>
</tbody>
</table>

Test environment
NEON-1020/ 2MP image size/ Intel Atom E3845 1.91GHz / Memory 4GB RAM

Figure 3. Despite the obvious benefits of cost, flexibility and performance, FPGA has not been as widely adopted in vision systems since its introduction in 1984. One major reason is difficulty in programming. Few programmers are familiar with the low-level languages used with FPGAs like VHDL or Verilog. This creates a barrier to expanded development and use.

**New Generation Smart Cameras with FPGA Solution**

With the emergence of new interface products and design tools, FPGA is gaining new market momentum. In order to overcome programming challenges, ADLINK offers a new generation smart camera carrying embedded image preprocessing on FPGA with a C++ programming environment, eliminating the requirement for familiarity with other languages to benefit from the advantages of FPGA.

With pre-installation of selected image preprocessing functions, including LUT, shading correction and Region of Interest (ROI) capability, the smart camera uses FPGA as a co-processor to offload CPU tasking. The FPGA connects to the image sensor device (camera), preprocesses raw image input and streams the preprocessed data to the CPU for more complex image analysis. Accordingly, speed and performance of the smart camera easily surpass that of its conventional counterparts. To further increase ease-of-use, APIs can enable system integrators or users to compile FPGA functions in the Microsoft Visual Studio environment using C++.

In summary, new generation smart cameras with FPGA overcome the challenges presented with larger footprint, advanced processing machine vision solutions with the following benefits:
• Multi-processor architecture of CPU and FPGA cooperatively processes tasks to maximize performance and speed based on the most effective size and cost structure available.

• FPGA supercharges image processing capabilities by migrating operations into a familiar and easy-to-use control environment to reduce conventional programming barriers.

• Optimum balance between size and performance is achieved by use of a higher grade CPU than conventional smart cameras, generating maximum performance from small form factors, simultaneously meeting requirements for performance, size and convenience.

Alex Liang

Alex Liang has spent more than a decade in the machine vision industry, mainly focused on original design manufacturing (ODM) for industrial cameras. Prior to his product management work, he also spent time in project management, channel management and even plant management. Mr. Liang has an MBA from Tamkang University in Taipei, Taiwan.